



PBL6002D

60 V PNP BISS loadswitch

Rev. 01 — 23 June 2005

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

1.2 Features

- Low V_{CEsat} (BISS) transistor and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

Table 1: Quick reference data

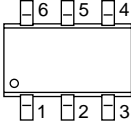
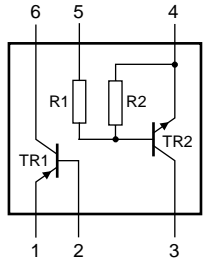
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current (DC)		[1]	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1$ A; $I_B = -100$ mA	[2]	255	340	m Ω
TR2; NPN resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Device mounted on a ceramic Printed-Circuit Board (PCB), Al_2O_3 , standard footprint.

[2] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

sym036

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
PBLS6002D	SC-74	plastic surface mounted package; 6 leads	SOT457

4. Marking

Table 4: Marking codes

Type number	Marking code
PBLS6002D	F2

5. Limiting values

Table 5: Limiting values

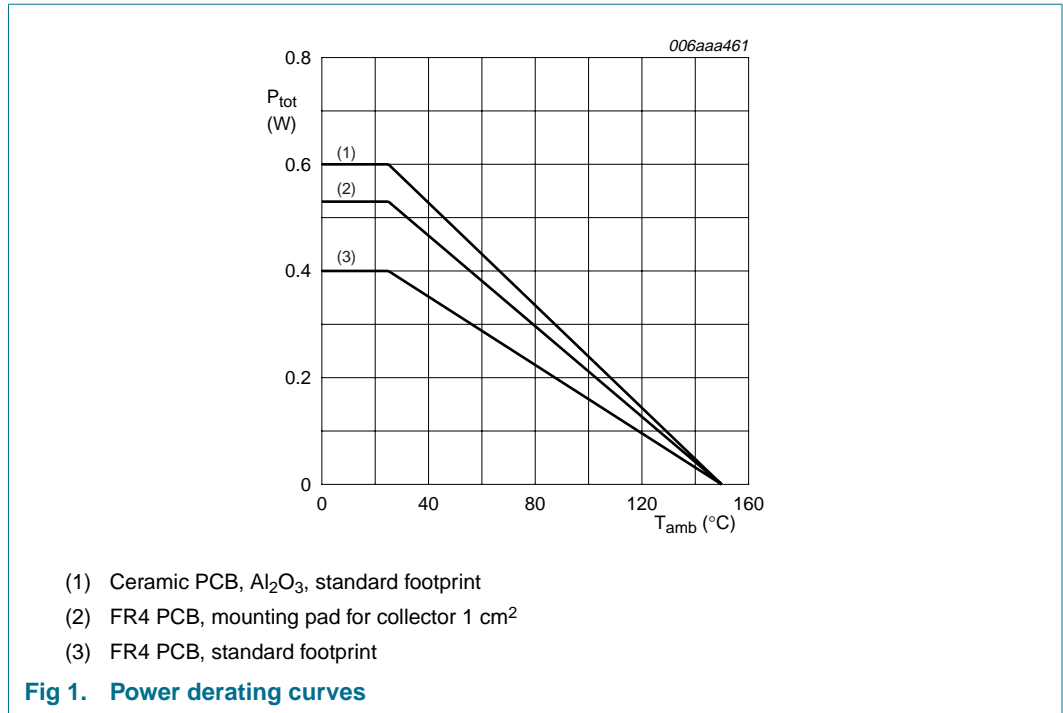
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter	-	-80	V	
V_{CEO}	collector-emitter voltage	open base	-	-60	V	
V_{EBO}	emitter-base voltage	open collector	-	-5	V	
I_C	collector current (DC)		[1]	-	-700	mA
			[2]	-	-850	mA
			[3]	-	-1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-2	A	
I_B	base current (DC)		-	-300	mA	
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	-1	A	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter	-	50	V	
V_{CEO}	collector-emitter voltage	open base	-	50	V	
V_{EBO}	emitter-base voltage	open collector	-	10	V	
V_I	input voltage					
			positive	-	+30	V
			negative	-	-10	V
I_O	output current (DC)		-	100	mA	
I_{CM}	peak collector current		-	100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
			[2]	-	200	mW
			[3]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	400	mW
			[2]	-	530	mW
			[3]	-	600	mW
T_{stg}	storage temperature		-65	+150	°C	
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-65	+150	°C	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	312	K/W
			[2]	-	-	236	K/W
			[3]	-	-	208	K/W
TR1; PNP low V_{CEsat} transistor							
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	105	K/W	

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

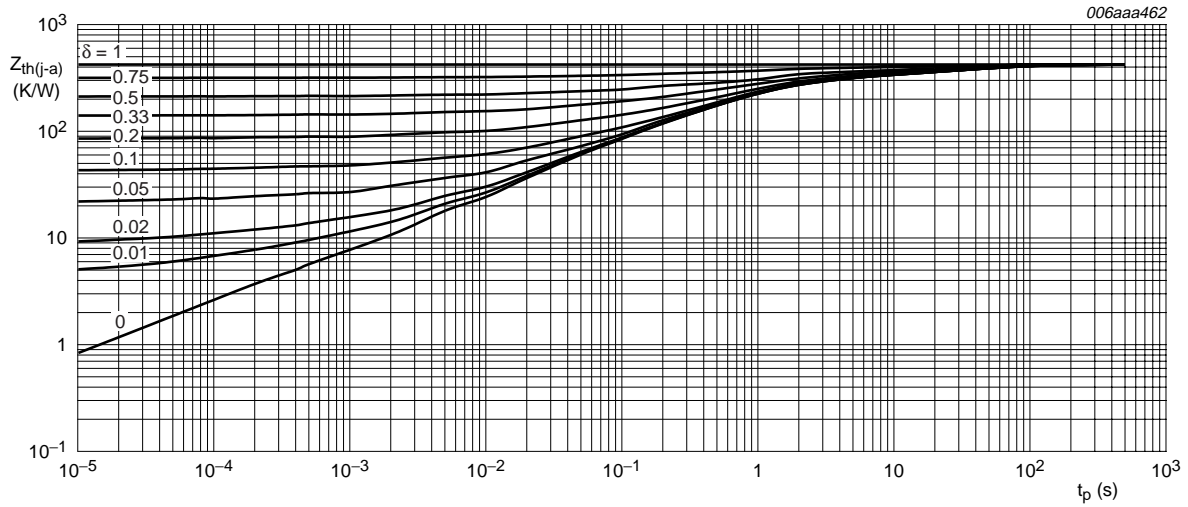


Fig 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values

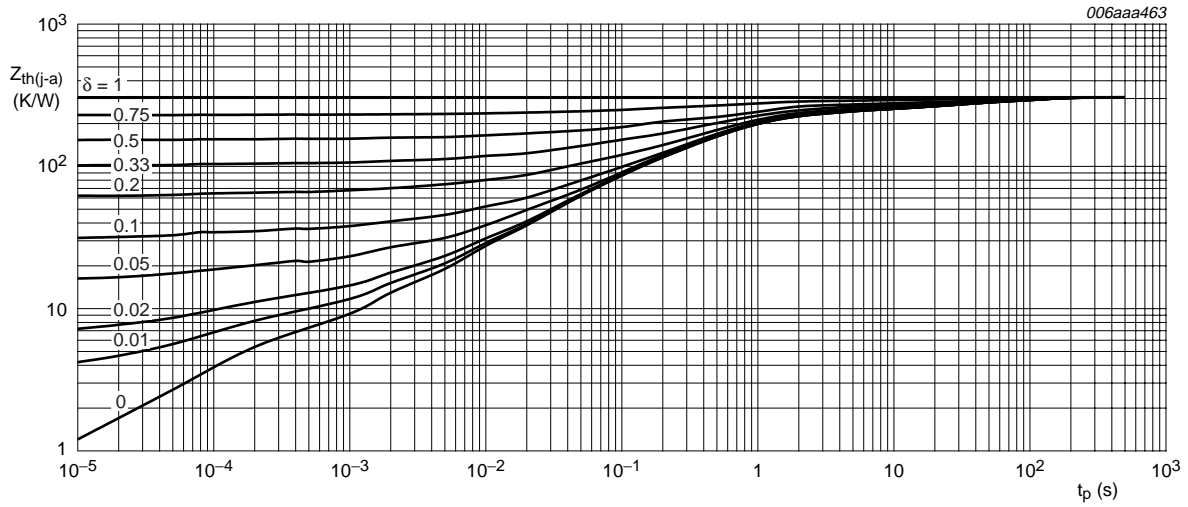
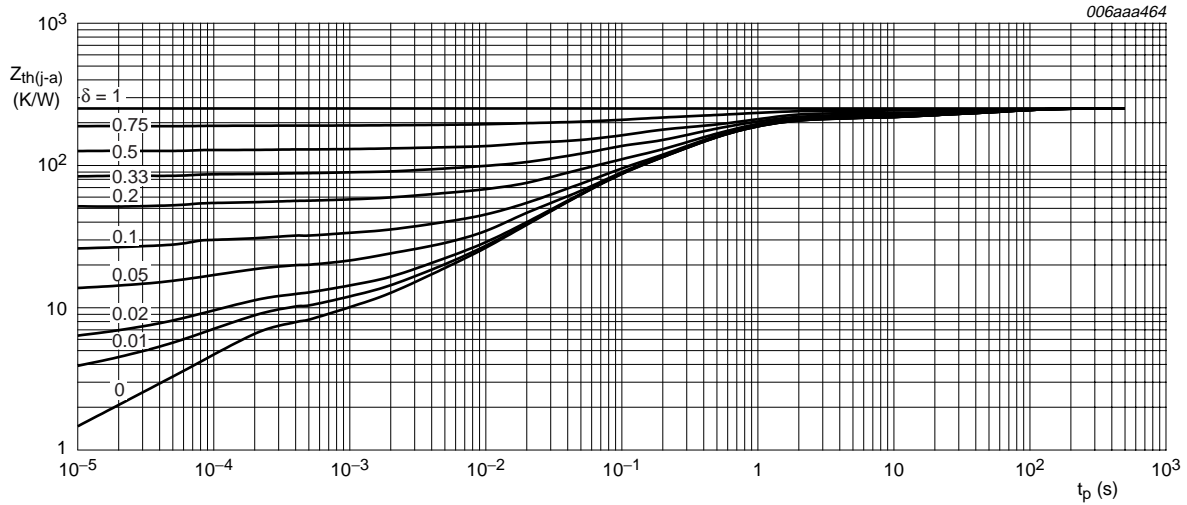


Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values

7. Characteristics

Table 7: Characteristics

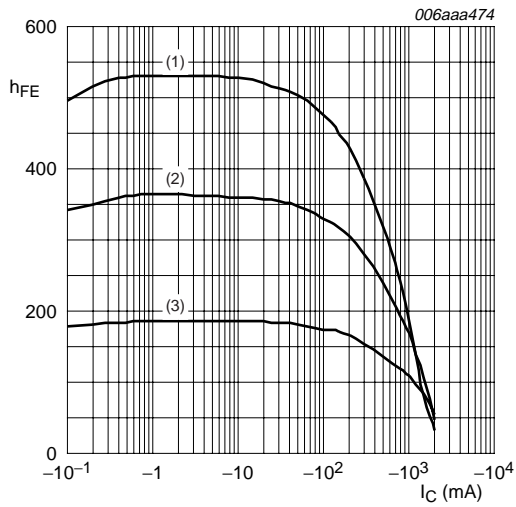
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = -60 V; I _E = 0 A	-	-	-100	nA
		V _{CB} = -60 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -60 V; V _{BE} = 0 V	-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -1 mA	200	350	-	
		V _{CE} = -5 V; I _C = -500 mA	[1] 150	230	-	
		V _{CE} = -5 V; I _C = -1000 mA	[1] 100	160	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -100 mA; I _B = -1 mA	-	-110	-175	mV
		I _C = -500 mA; I _B = -50 mA	[1] -	-135	-180	mV
		I _C = -1000 mA; I _B = -100 mA	[1] -	-255	-340	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -100 mA	[1] -	255	340	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -1 A; I _B = -50 mA	[1] -	-0.95	-1.1	V

Table 7: Characteristics ...continued
 $T_{amb} = 25^\circ\text{C}$ unless otherwise specified.

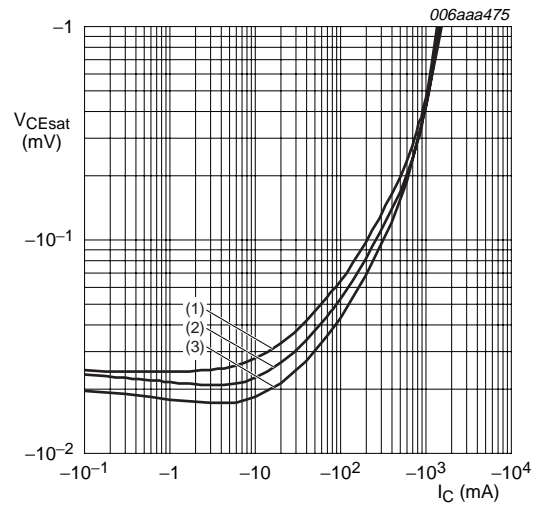
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}; I_C = -1\text{ A}$	[1] -	-0.82	-0.9	V
t_d	delay time	$I_C = -0.5\text{ A};$	-	11	-	ns
t_r	rise time	$I_{Bon} = -25\text{ mA};$	-	30	-	ns
t_{on}	turn-on time	$I_{Boff} = 25\text{ mA}$	-	41	-	ns
t_s	storage time		-	205	-	ns
t_f	fall time		-	55	-	ns
t_{off}	turn-off time		-	260	-	ns
f_T	transition frequency	$I_C = -50\text{ mA};$ $V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	150	185	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V};$ $I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	9	15	pF
TR2; NPN resistor-equipped transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A};$ $T_j = 150^\circ\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	900	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 20\text{ mA}$	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA};$ $I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V};$ $I_C = 20\text{ mA}$	2.5	1.9	-	V
R1	bias resistor 1 (input)		3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V};$ $I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	2.5	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.



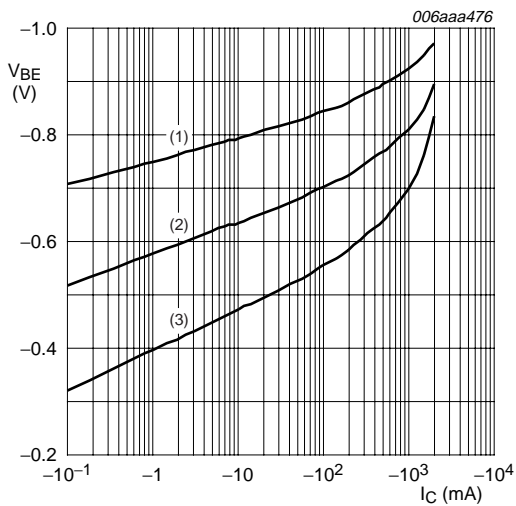
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -55\text{ }^\circ\text{C}$

Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values



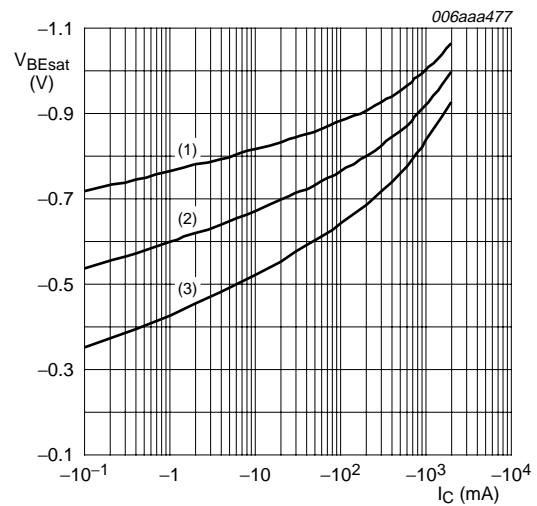
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -55\text{ }^\circ\text{C}$

Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



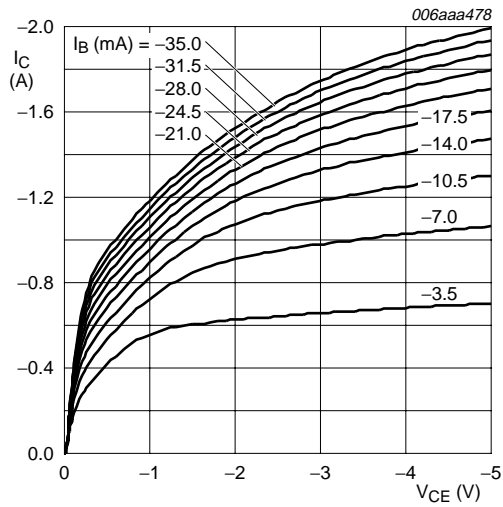
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = -55\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



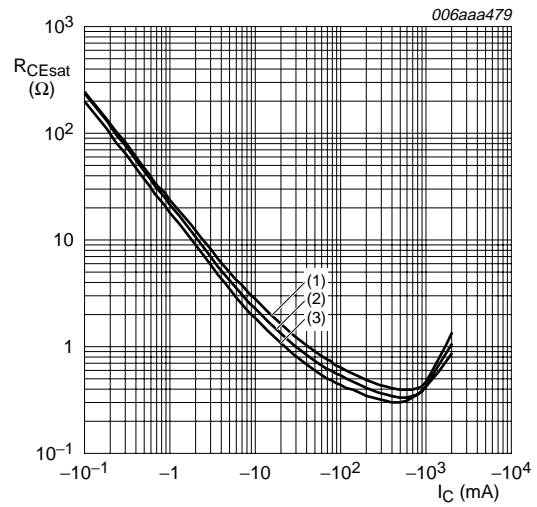
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$

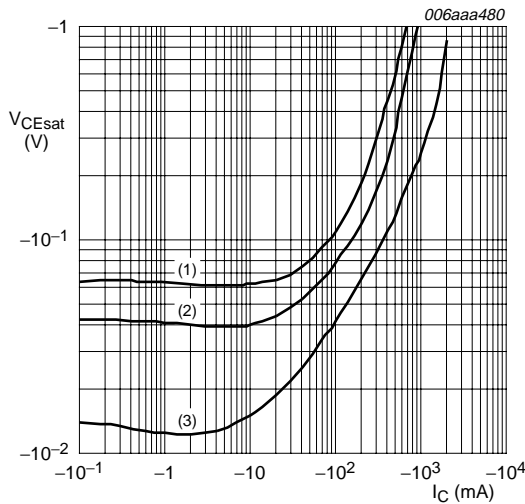
Fig 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



$I_C/I_B = 20$

- (1) $T_{amb} = 100\text{ }^\circ\text{C}$
- (2) $T_{amb} = 25\text{ }^\circ\text{C}$
- (3) $T_{amb} = -55\text{ }^\circ\text{C}$

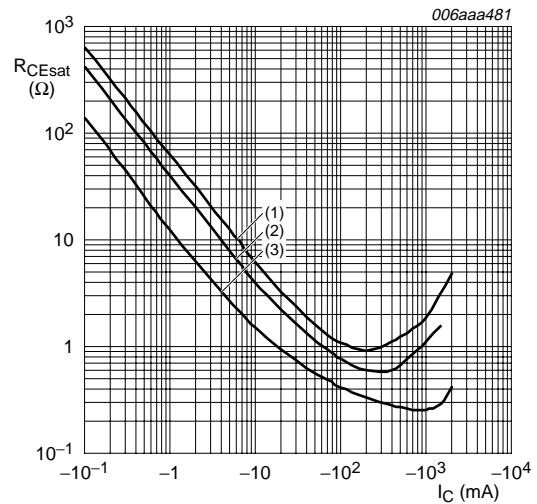
Fig 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

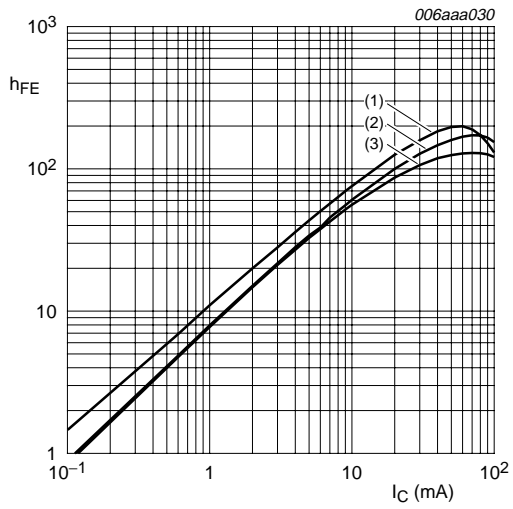
Fig 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$T_{amb} = 25\text{ }^\circ\text{C}$

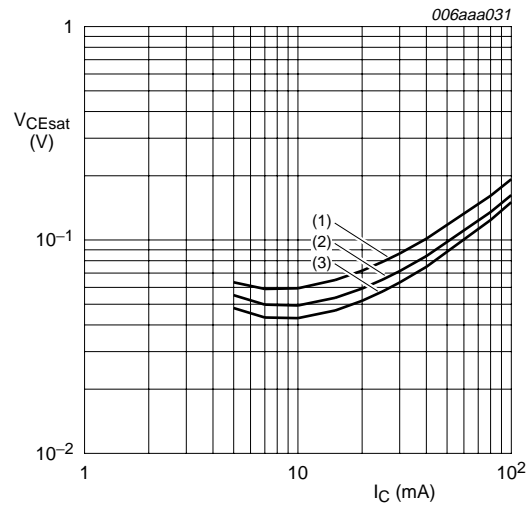
- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



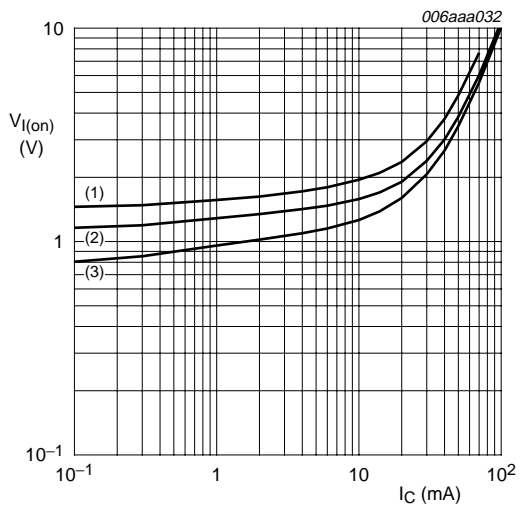
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 150^\circ\text{C}$
 (2) $T_{amb} = 25^\circ\text{C}$
 (3) $T_{amb} = -40^\circ\text{C}$

Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values



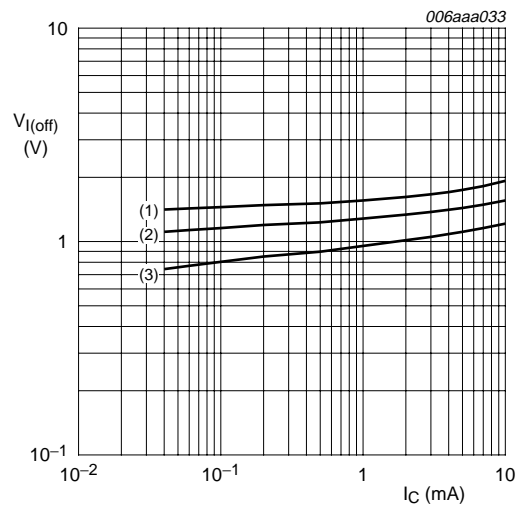
$I_C/I_B = 20$
 (1) $T_{amb} = 100^\circ\text{C}$
 (2) $T_{amb} = 25^\circ\text{C}$
 (3) $T_{amb} = -40^\circ\text{C}$

Fig 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40^\circ\text{C}$
 (2) $T_{amb} = 25^\circ\text{C}$
 (3) $T_{amb} = 100^\circ\text{C}$

Fig 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40^\circ\text{C}$
 (2) $T_{amb} = 25^\circ\text{C}$
 (3) $T_{amb} = 100^\circ\text{C}$

Fig 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

8. Test information

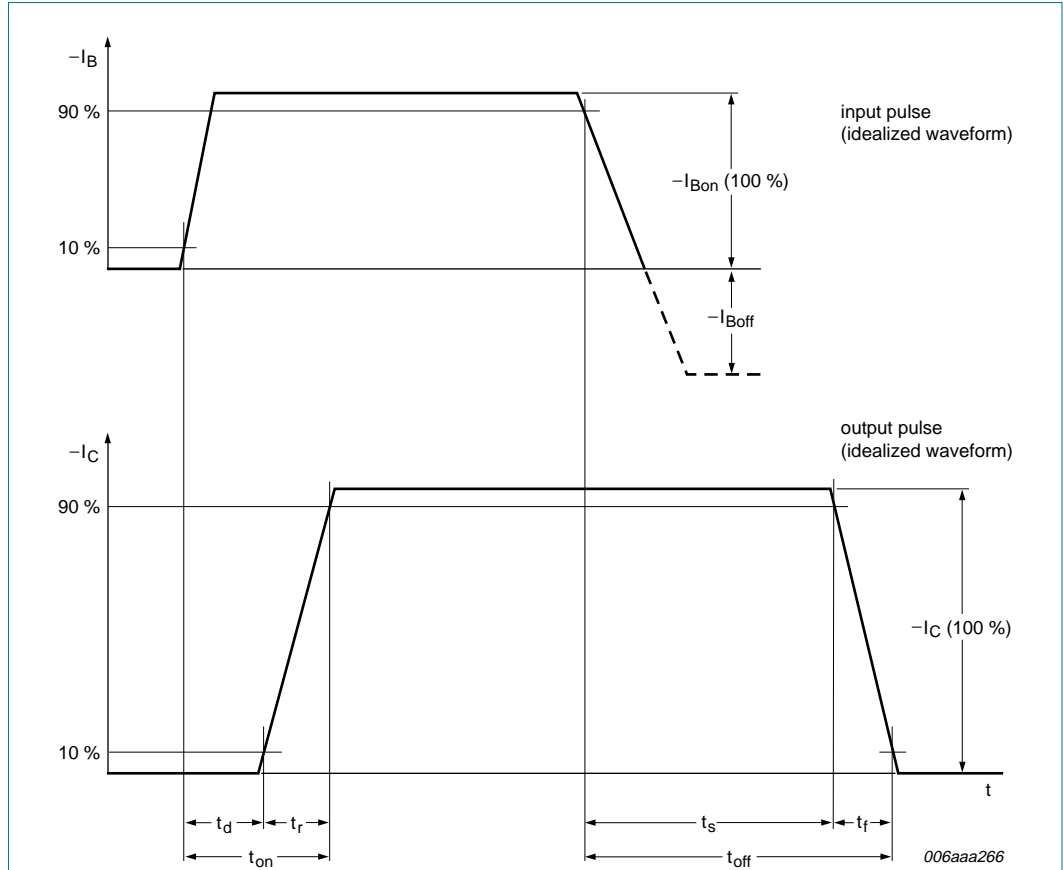
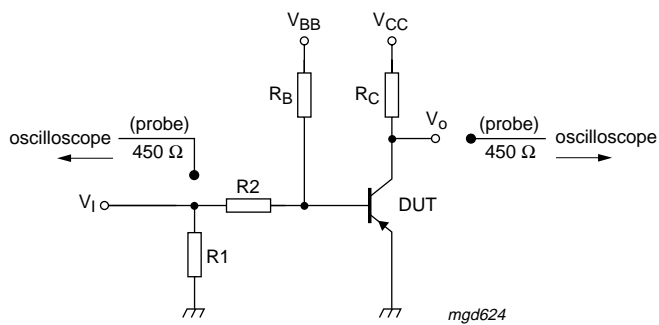


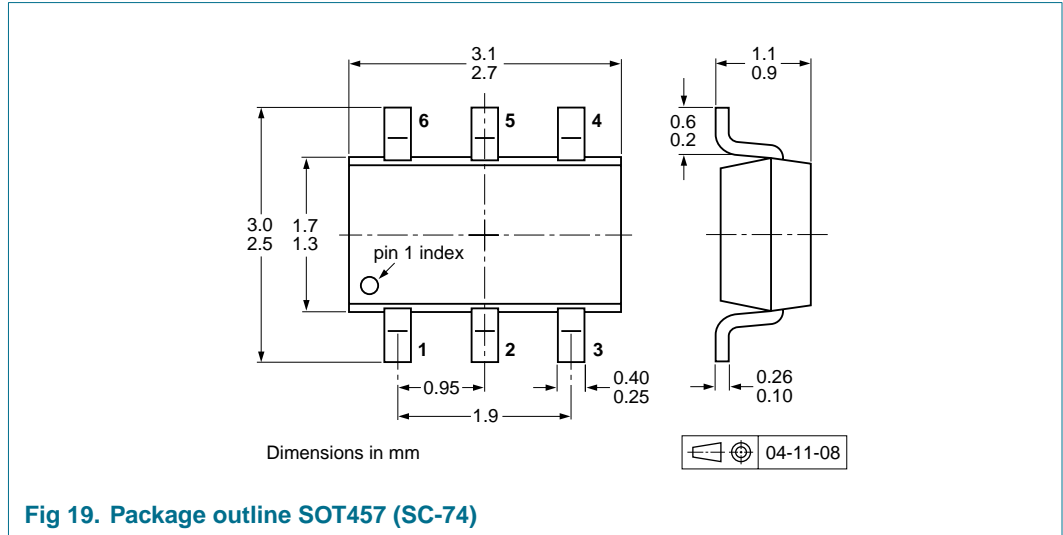
Fig 17. BISS transistor switching time definition



$I_C = -0.5$ A; $I_{Bon} = -25$ mA; $I_{Boff} = 25$ mA; $R_1 =$ open; $R_2 = 100$ Ω ; $R_B = 300$ Ω ; $R_C = 20$ Ω

Fig 18. Test circuit for switching times

9. Package outline



10. Packing information

Table 8: Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

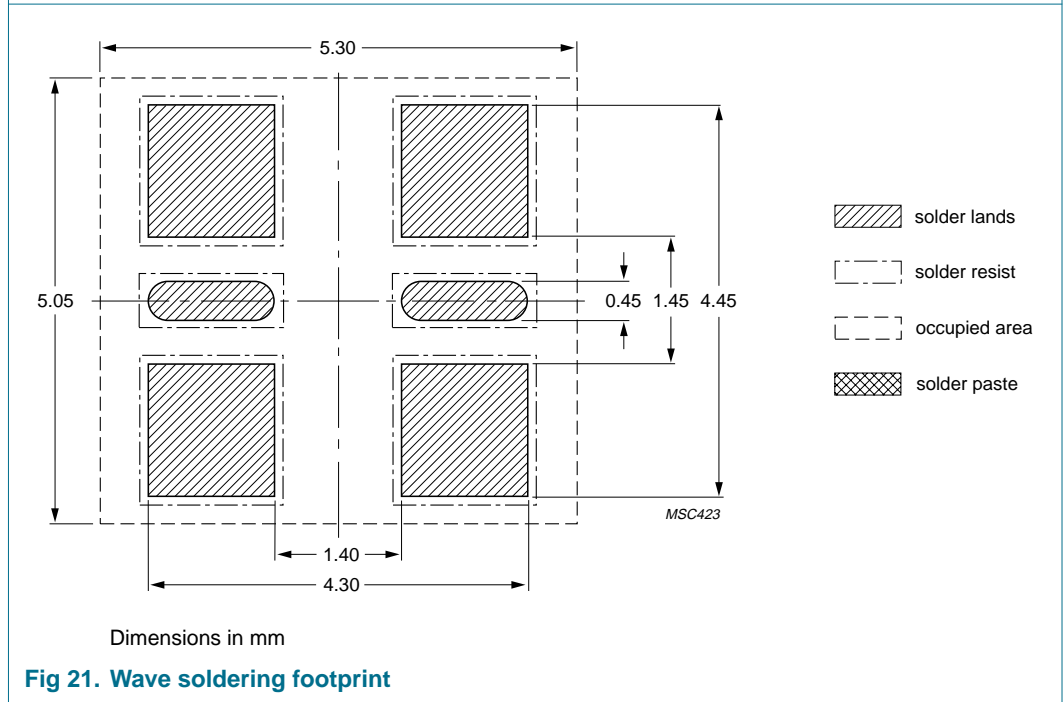
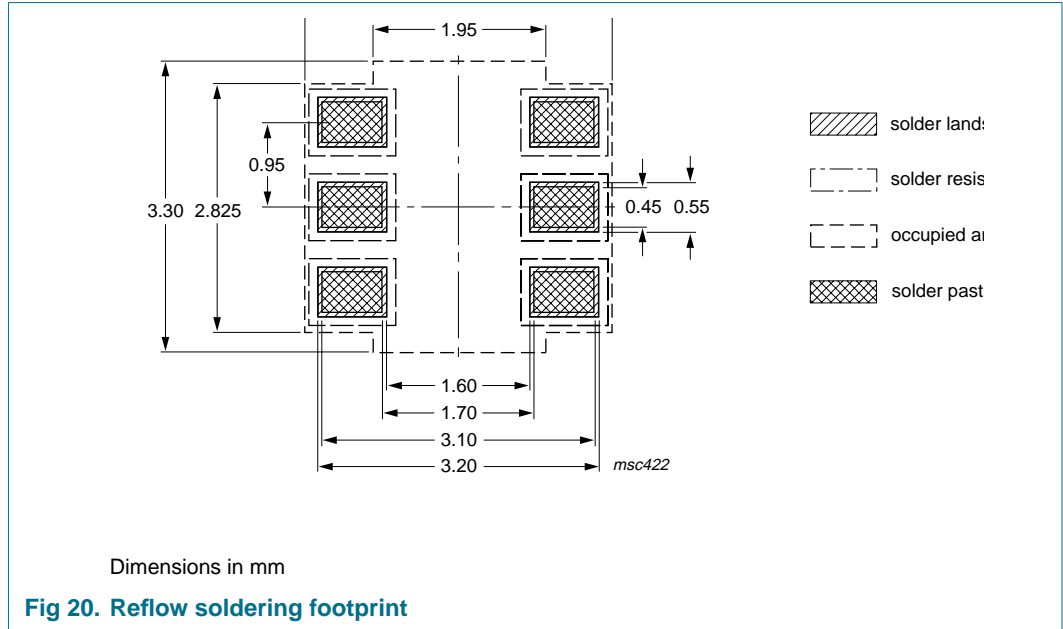
Type number	Package	Description	Packing quantity	
			3000	10000
PBLS6002D	SOT457	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-165

[1] For further information and the availability of packing methods, see [Section 17](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering





12. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PBLS6002D_1	20050623	Product data sheet	-	9397 750 15197	-

13. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

14. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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17. Contact information

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